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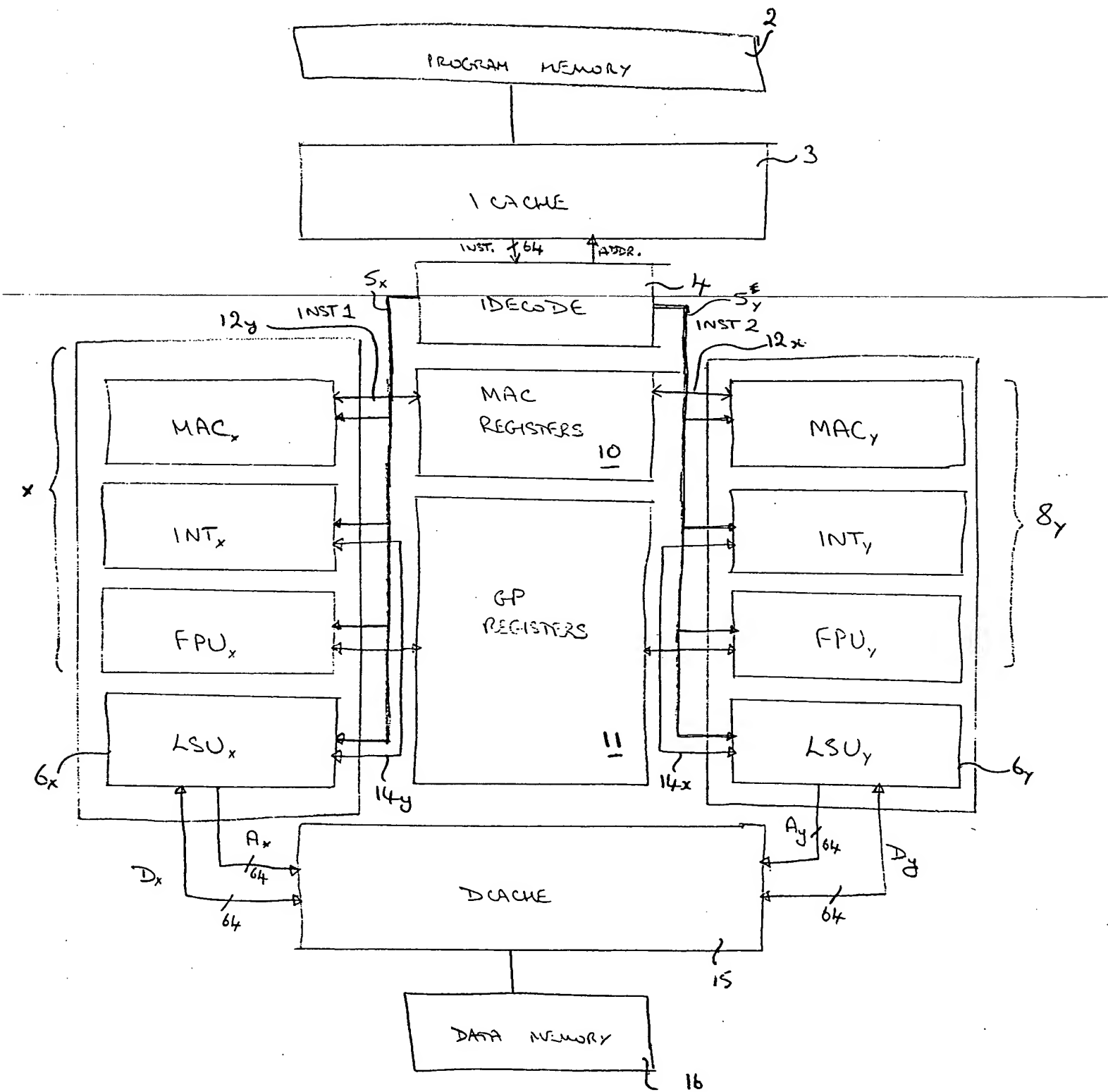


Figure 1

Figure 3

1D bit



31   30   29   28   27   26   25	24   23   22   21   20   19   18	17   16   15   14   13   12   11	10   09   08   07   06   05   04	03   02   01   00	
M   G   OPCODE	S   TST   SRC2	SRC1	DST	(1)	
M   G   OPCODE	TST   IMMED	SRC1	DST	(2)	
M   G   OPCODE	S   TST   SRC2	SRC1	SIGN   M REG	(3)	
M   G   OPCODE	S   TST   SHIFT   M REG	SRC1	DST	(4)	
M   G   OPCODE	S   TST   SRC2	SRC1	DST	(5)	
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M   OPCODE	INDX OP   T   INDX REG	BASE REG	DST	(7)	

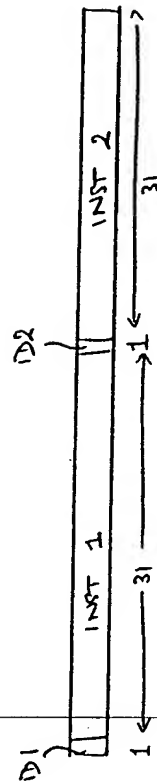
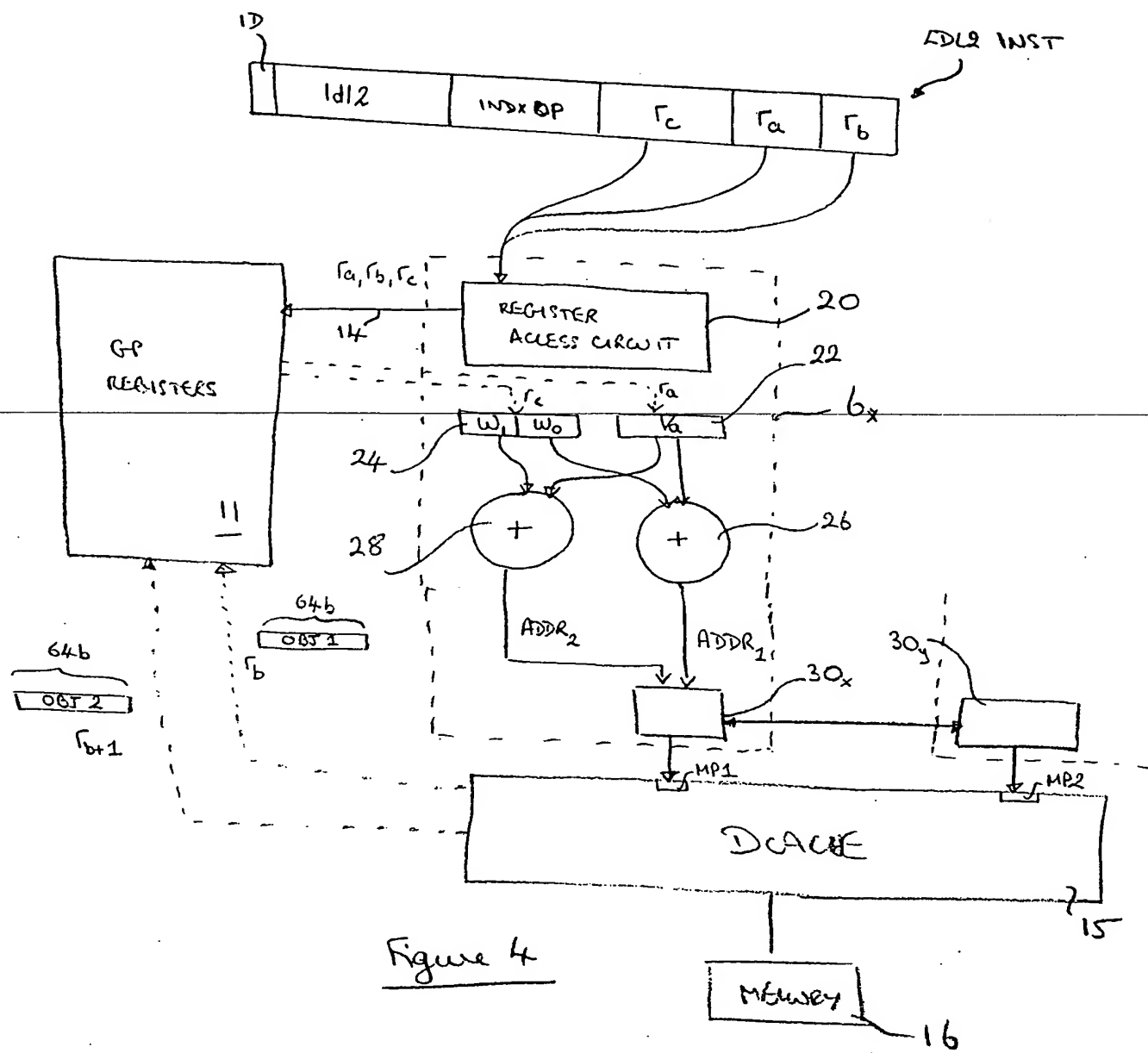


figure 2



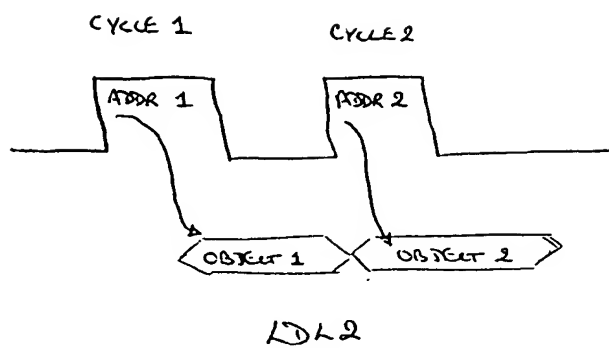


Figure 5a

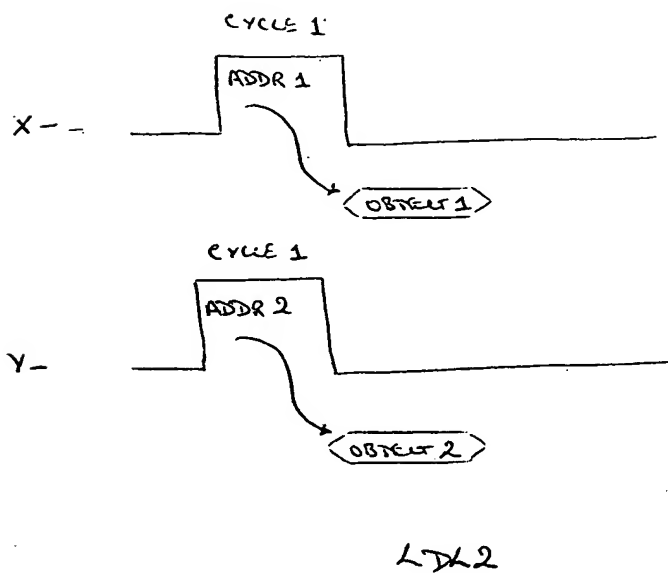


Figure 5b

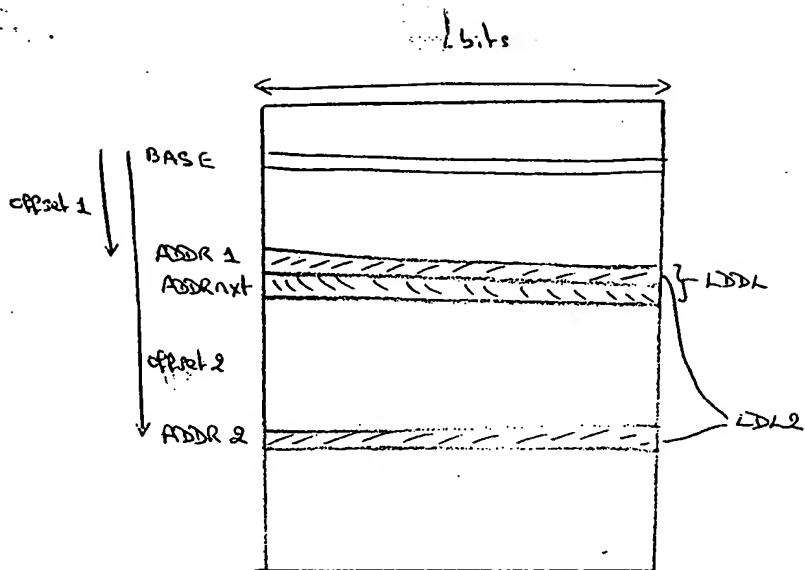


Figure 6

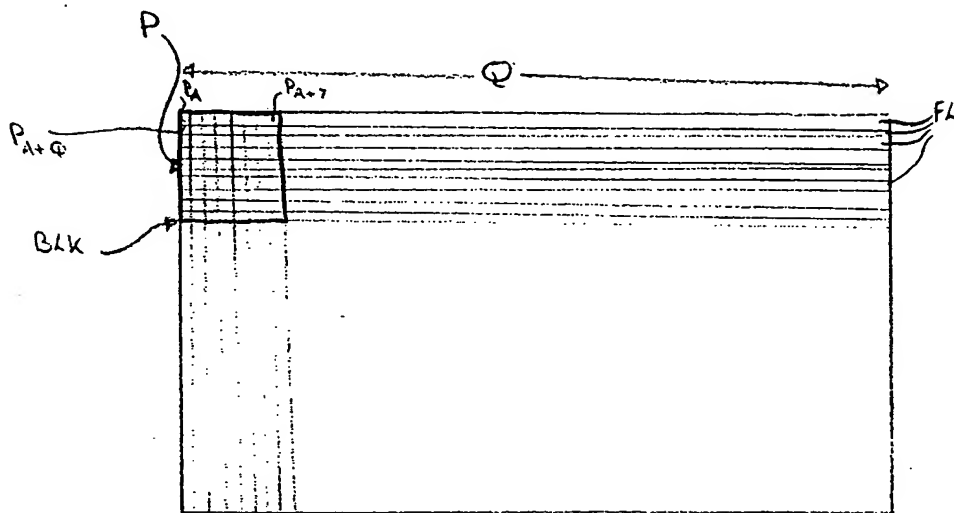


Figure 7

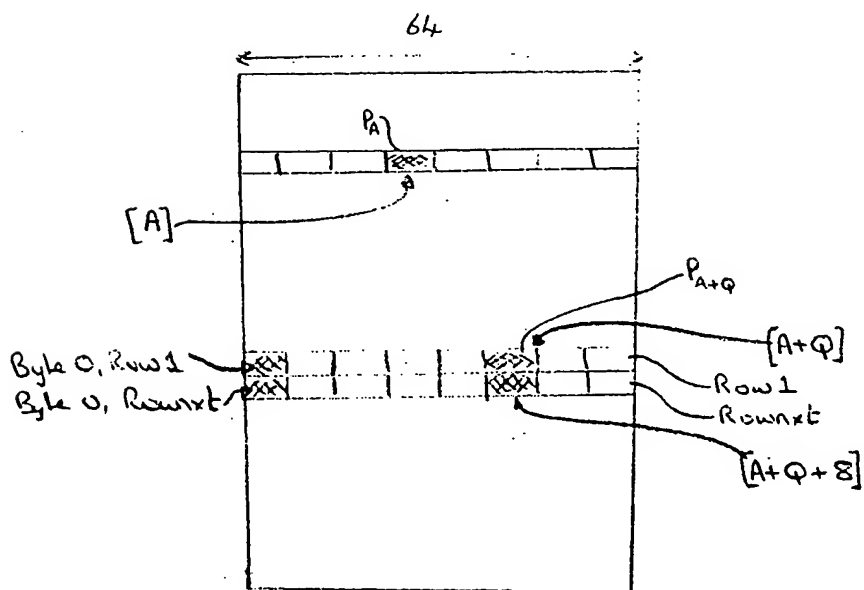


Figure 8